Behavioral Comparison of the Sampling Cycle of Three 12-bit SAR ADC Architectures and 500kHz Clock in CMOS Technology

Willian Mateus Ramthun
Electrical Engineering
Universidade do Constestado
Canoinhas, Brazil
willian_ramthun@ieee.org

Igor José langer
Electrical Engineering
Universidade do Contestado
Canoinhas, Brazil
i-langer@ieee.org

Luis Edaurdo Palomino Bolivar
Electrical Engineering
Universidade do Contestado
Canoinhas, Brazil
palomino@unc.br

***Abstract*—In this paper are proposed three 12-bit resolution successive-approximation register (SAR) for analog and digital converter (ADC) architectures, with the objective of comparing the Sampling Cycle mode with a new ADC architecture called Pre-Load ADC. To compare the sampling speed increase, the ADC internal comparison signal used in DAC R-2R was changed during comparisons. The conversion cycle speed increase of 10 times stands out when employing CMOS commercial model, with 2V polarization, 0.5872 V best V_{RMS} and 500kHz clock.**

Keywords—SAR ADC, Sample, DAC, ADC, Conversion.

I. INTRODUCTION

Conversion circuits are fundamental stages in electrical systems, they convert analog into digital signals (ADC) [1]. Currently there are many works which present ADC techniques and topologies like the one reported in [2]. The input voltage signal or frequency signal (FDC), once digitalized are treated in a digital signal processing (DSP) unit. Therefore, signals are converted from digital to analog (DAC) or in frequency (DFC), as similar in Fig 1.

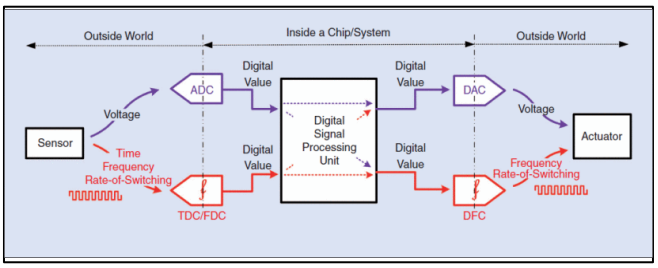

Fig. 1.Processing flow in DSP enabled by ADC or TCD in input and DAC or DFC in output. [1].

Fig. 2 presents a Successive-Approximation-Receiver (SAR) ADC. These are mainly employed to increase the bit resolution and in Nyquist sampling rate frequencies between 1MHz and 900MHz [3]. The SAR ADC, are used in a wide range of electronic circuits, e.g. they are found in RF transceiver integrated circuit projects, in the phase that determines the interpretation sensibility of I and Q codes from the demodulation, prior to the digital module or Digital Signal Processing and consequently making it important for any telecommunication project [4]. The efforts made to improve the precision and the speed of respond of ADCs, can be see in [5], for which the SAR ADC improves the control of the Voltage Controller Oscillator.

All three 12-bit SAR ADC models presented here have the same configuration, all having: the DAC R-2R module; 500kHz clock and the same sinewave as the input signal. The quantization characteristic is uniform, and offset is zero [6].

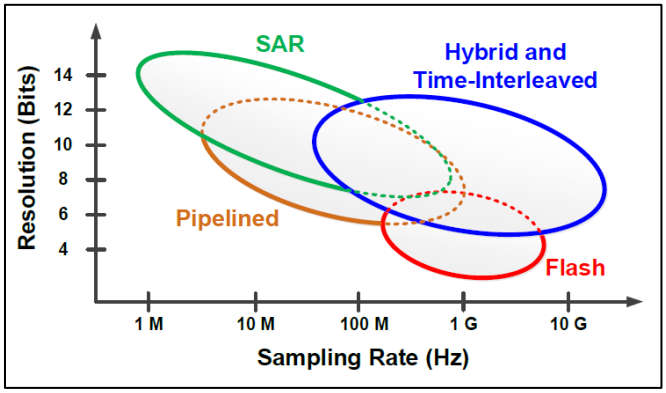

Fig. 2.Overview of Nyquist-rate ADC operation ranges.

II. SAR ADC MODELS

The SAR ADC architecture presented in Fig. 3, describes the simplified form of the modules it consists of. Its operation is based on comparison of an input analog signal and another signal in a TRACK/HOLD (TH) circuit. The TH circuit samples and holds de voltage of the analog input *Analog IN*, with full-scale is V_{REF} [7]. The V_{REF} is the DAC voltage reference, define the voltage range, in which the ramp is generated too. The R2-R DAC engenders a *N*-bit signal for each sample ramp generated by the N-BIT REGISTER block, and once $V_{DAC} > V_{IN}$, the comparator refeeds the control signal to the SAR LOGIC, which holds the N-BIT REGISTER state, outputting the conversion value in serial or parallel. The sampling frequency is determined by the N-BIT REGISTER, where every ramp step is equivalent to a clock period.

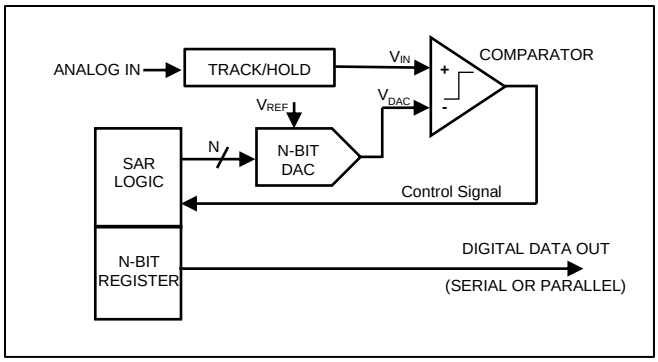

Fig. 3.Simplified N-bit SAR ADC architecture.

A. Basic architecture

The Fig. 4 presents the basic 12-bit resolution SAR ADC architecture, employing a R-2R DAC. In this proposal, the registers hold the SAR LOGIC value once the comparator indicates $V_{DAC} > V_{IN}$. In this case the comparison value is kept until the DAC analog waveform cycle V_{DAC} is completed, therefore the response time to start a new conversion is determined in (1), where N is the number of bits, and F_{CLK} is the SAR LOGIC input clock frequency. Thus T_{SAMPLE} = 81.9 ms. In this architecture the control signal establishes the SAR LOGIC digital information capture timing. The values: N = 12, V_{IN} = 0.5V, V_{REF} = 2V, F_{CLK} = 500kHz and T_{SAMPLE} (V_{IN}) = 8.19 ms.

$$T_{SAMPLE} = \frac{2^N}{F_{CLK}} \qquad (1)$$

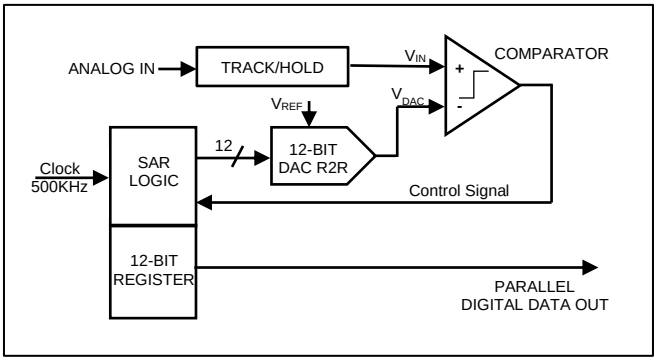

Fig. 4.Basic 12-bit SAR ADC architecture, 500kHz and R-2R DAC.

B. Architecture with reset

The SAR ADC displays a DELAY block as shown in Fig. 5. It is used to delay the comparator control signal because it is a SAR LOGIC reset signal. Thereby, the reset is generated by the VDAC after the capture of the digital values in the 12-BIT REGISTER.

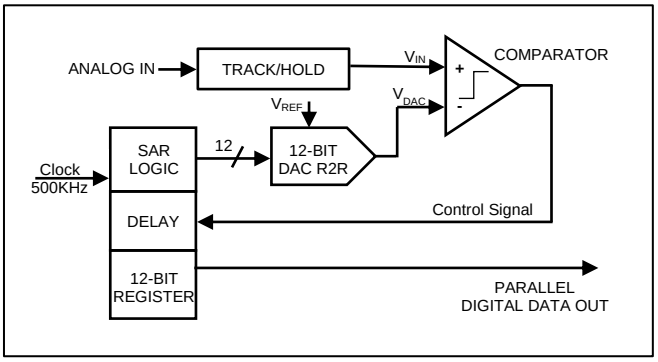

Fig. 5.SAR ADC architecture with reset.

The SAR LOGIC reset effect allows the V_{DAC} signal period to be variable according to the V_{IN} amplitude, as shown in Eq. (2). The sampling time T_{SAMPLE} is in function of V_{IN}, for this case the values of ADC: N = 12, V_{IN} = 0.5V, V_{REF} = 2V, F_{CLK} = 500kHz and $T_{SAMPLE}(V_{IN})$ = 2.05 ms.

$$T_{SAMPLE}(V_{IN}) = \frac{V_{IN} \cdot 2^N}{V_{REF} \cdot F_{CLK}} \qquad (2)$$

C. Architecture with pre-load

The SAR ADC with pre-load as presented in Fig. 6 has a PRE-LOAD block, which allows to define a start value to V_{DAC} signal, as consequence it denies the SAR LOGIC to generate a signal that starts in zero or the reset value. The control signal of this architecture prevents the generation of the signal from V_{DAC} to V_{REF} value. As indicated in Eq. (3), the initial position of the comparison signal VDAC is placed considering the last conversion value in the 12-BIT REGISTER located in the Parallel-Digital-Data-Out (PDDO). This PDDO starting point accounts for a pre-load value (VPL), which approaches V_{DAC} to V_{IN} voltage value, thus the comparison value $V_{DAC} > V_{IN}$ is achieved quickly and the time value of T_{SAMPLE} is lower.

$$T_{SAMPLE}(V_{IN}) = \left(\frac{V_{IN}}{F_{CLK}} - PDDO[n-1]\right) \cdot \frac{2^N}{V_{REF}} + V_{PL} \qquad (3)$$

For values of N = 12, V_{IN} = 0.5V, V_{REF} = 2V, F_{CLK} = 500kHz a previous PDDO conversion value is considered: $PDDO[n-1]$ = 0.5 $T_{SAMPLE}(V_{IN})$ = 6 µs.

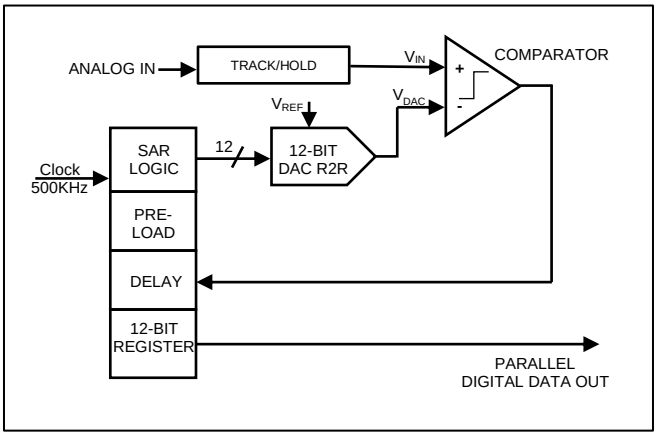

Fig. 6. Basic 12-bit SAR ADC architecture, 500kHz and R-2R DAC.

III. Circuits Simulation

The validation of the operational model is proposed with a simulation of each SAR ADC described in this paper, which all are employing PSPICE in Multisim. The simulation components are CMOS, identifying in each circuit the architecture elements matching with the previous one, and utilizing a R-2R DAC in the registers output to compare the PDDO signal with the V_{IN} input signal. The V_{REF} = 2V is equal to the polarization value of the devices and using a 500kHz clock signal.

The 74HC family counters are employed in schematics, with 2V polarization, comprising SAR LOGIC blocks with three counters 74HC191, the DELAY using five *not* gates 74HC04, two 12-BIT R-2R DAC with 10 Ω and 20 Ω resistors, the 12-BIT REGISTER with three 74HC194, the PRE-LOAD with three 74HC283, the TRACK/HOLD was implemented in the input source V_{IN}, and the COMPARATOR with a LM339.

For each architecture, the simulation shown the SAR ADC schematic and COMPARATOR input values V_{IN} and V_{DAC}. The output system is *Y[n]*, which takes signal in alternative DAC transforming 12 Bit PDDO in unique discrete line and the obtained signals in each proposed, with the error being determined by the relation between the input signal V_{IN} and the *Y[n]* output, according to Eq. (4), where *t* is time.

$$Error(t) = V_{IN}(t) - Y[n] \quad (4)$$

A. *Basic architecture SAR ADC simulation*

Fig. 7 shows the basic architecture SAR ADC circuit with the control signal connected to the comparator and the clock command in the 12-BIT REGISTER, thereby the signal generated by the SAR ADC is converted in the 12-BIT R-2R DAC (V_{DAC}) and then compared to the ANALOG IN signal (V_{IN}). As shown in Fig. 8, the V_{DAC} signal travels from 0V to the V_{REF} value, thus the signal sampling frequency being 10 samples every 2 µs.

The error shown in Fig. 8 is inside a voltage range between -0.5 V and 0.5 V, therefore V_{PP} = 1 V with its frequency being equivalent to V_{IN} frequency.

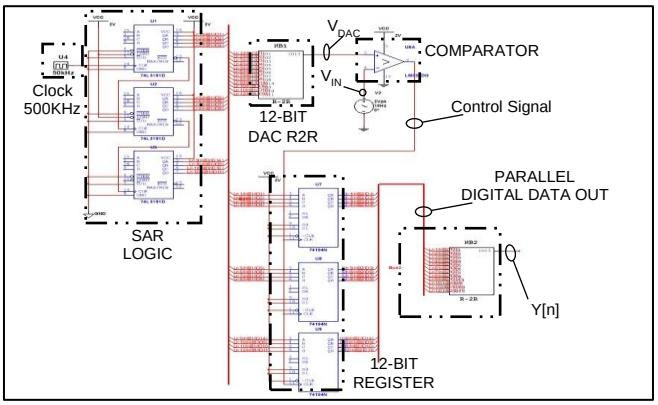

Fig. 7.Basic SAR ADC schematic with functional device CMOS

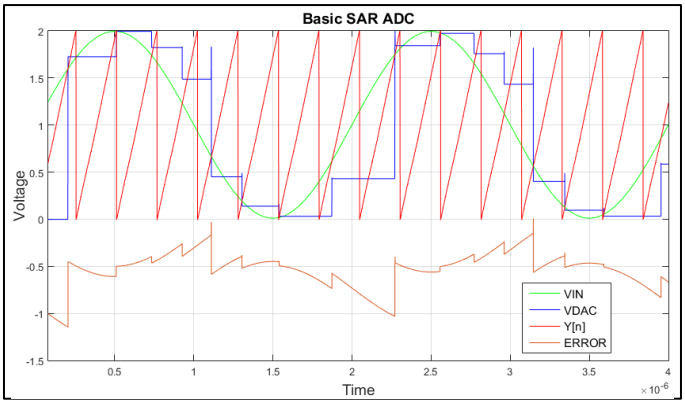

Fig. 8.Signals characteristics of basic SAR ADC with error (Offset = -1 V).

B. *Reset SAR ADC architecture simulation*

Fig. 9 illustrates the reset SAR ADC circuit with the DELAY module implemented in the bottom right corner of the figure. The control signal triggers the SAR LOGIC signal reading in the 12-BIT REGISTER and delays the generation of another sampling cycle in the DELAY. Thereby the 12-BIT R-2R DAC output in V_{DAC} is compared to the ANALOG IN signal (V_{IN}), leading to a new conversion if the $V_{DAC} > V_{IN}$ condition is achieved. The delayed time is adjusted to be enough to read the registers.

As shown in Fig. 10, the V_{DAC} signal travels from 0V to the value of V_{IN}, thus making the signal sampling frequency reach 25 samples every 2µs. The error is between -0.5V and 0.5V range, and V_{PP} = 1V, there are some intrinsic glitches to the commutation of digital devices.

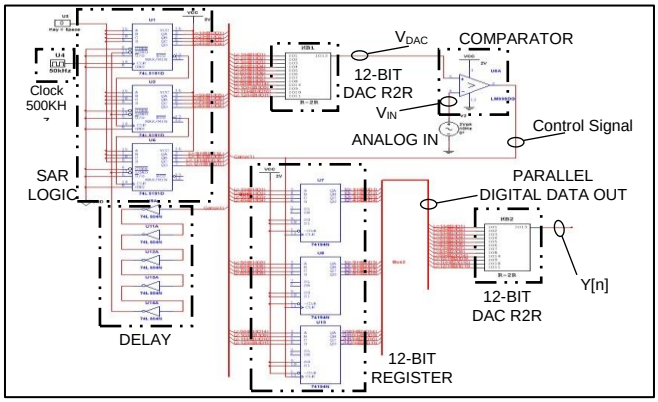

Fig. 9. Reset SAR ADC schematic with functional device CMOS.

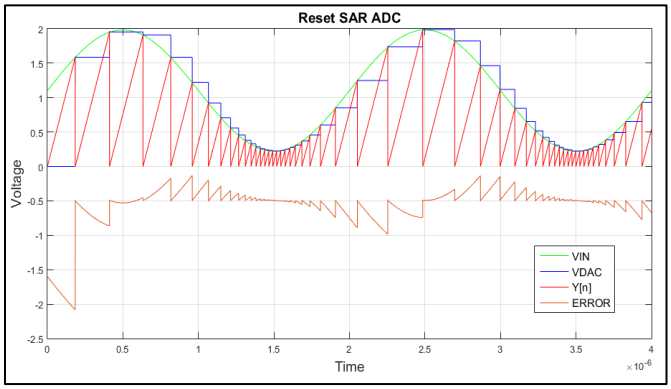

Fig. 10. Signals characteristics of Reset SAR ADC with error (offset = -1 V).

C. *Pre-Load SAR ADC architecture simulation*

The Pre-Load SAR ADC architecture schematic, presented in Fig. 11, adds a PRE-LOAD module configured by a subtractor, which decrements the converted value in the *Y[n]* in 125 or 3FH, highlighting the voltage (V_{DAC}) starting point in the simulation for each sampling cycle. Therefore, the PRE-LOAD (*Y[n] – 3FH*) resulting value is loaded in the SAR LOGIC, initiating the SAR ADC successive sums with this value.

This SAR ADC model also advantages the aspect of initiating the sampling cycle after the $V_{DAC} > V_{IN}$ condition is fulfilled and delayed signal for take a digital value and loads the SAR LOGIC counters with near value to V_{IN}.

Fig. 12 shows simulation results, highlighting the quantity of samples, once V_{DAC} keeps up with the input waveform V_{IN}. Thus, the *PDDO* is a high sampling rate signal, in this case 100 samples every 2µs. The inherent error in this architecture is 0.4V V_{PP}, and it is generated by the sampling cycle restart condition, once the V_{IN} is reached.

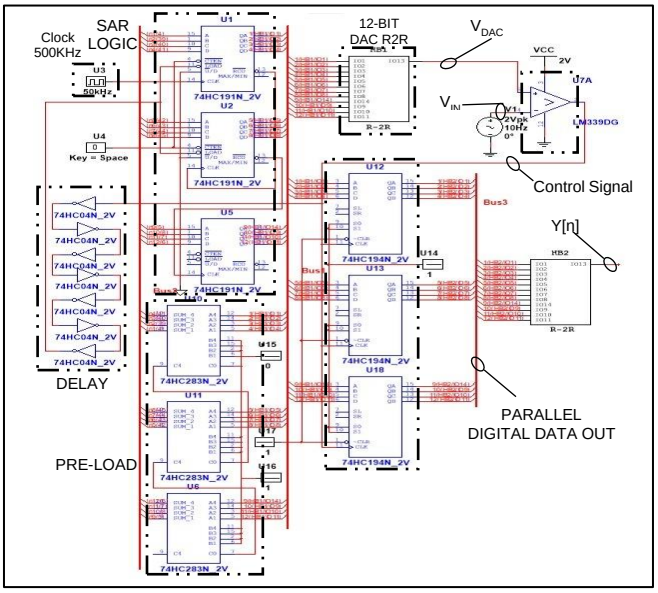

Fig. 11.Pre-Load SAR ADC schematic with operational CMOS device.

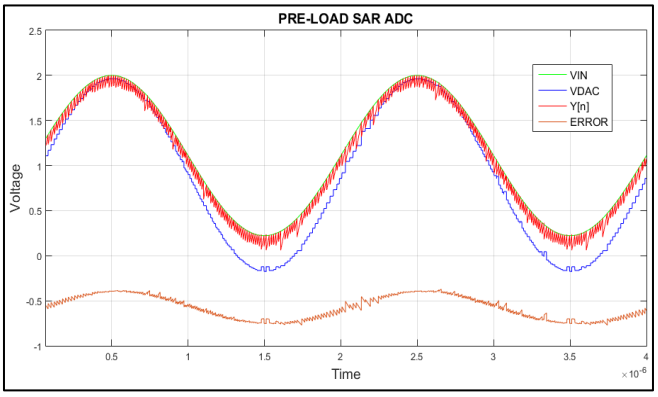

Fig. 12.Signals characteristics of Pre-Load SAR ADC with error offset = -1 V.

The values acquired with the SAR ADC architectures are shown in the TABLE I. The energy consumption is determined analyzing the polarization current in the modules and taking the Pre-Load architecture as reference.

TABLE I. SAR ADC DISCRETE ARCHITECTURE COMPARISON

SAR ADC ARCHITECTURES (500 KHz Clock)					
Architecture	***Qty of Devices***	***Samples 2µs***	***Energy Consume***	***Error RMS***	***Error V_{PP}***
Basic	9	10	70%	1.1375	1
Reset	10	25	75%	0.7326	0.7
Pre-Load	13	100	100%	0.5872	0.4

All values shown in TABLE I for Pre-Load SAR ADC type have more device and hence more energy consumption, but error is 60% least than other architectures. The SAR ADC type Reset and Basic is near to energy consume but the error is 30% improved although only one delay module.

The other hand the quantity samples in 2 µs done by the Pre-Load SAR ADC, make 10 times more than a Basic SAR ADC and 4 times more that Reset SAR ADC.

IV. COMMENTARIES

The Reset SAR ADC operation demonstrates an improvement when compared to the basic model, which uses *not* gates arrangement working as a delay, but having a lower complexity level if compared to the Pre-Load architecture. The TABLE I illustrates a conversion speed increase with just one parameter V_{PL} achieving up to 10 times more samples than the basic SAR ADC.

This research shows the technical viability for development of a new ADC type, proposed with Pre-Load SAR ADC in an integrated circuit. It is intended the production of 130nm prototypes of this circuit in 12 Bit resolution. Although assembling a converter with a programmable Pre-Load is considered necessary, likewise the considerations about the R-2R DAC architectures with negative V_{REF} and comply with technical restrictions of the telecommunications standards. The quantization error is not uniform, but calibration and linearity can obtain better results of performance.

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V. REFERENCES

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